Resistor R1 and capacitor C2 are connected in series in a line 57 extending to one of the fixed contacts of a relay 58. The coil 59 of relay 58 is connected between line 53 and a line 61 which extends from the moving contact of the relay to the common negative line 54 via a normally closed pressure operated switch 62. The pressure control line 63 of switch 62 is connected in a manner to be described below to a gas collection chamber of electrolytic cell 41 in order to provide a control connection whereby switch 62 is opened when the gas in the collection chamber reaches a certain pressure. However, provided that switch 62 remains closed, relay 58 will operate when ignition switch 48 is closed to provide a connection between lines 57 and 61 thereby to connect capacitor C2 to the common negative line 54. The main purpose of relay 58 is to provide a slight delay in this connection between the capacitor C2 and the common negative line 54 when the circuit is first energized. This will delay the generation of triggering pulses to thyristor T1 until a required electrical condition has been achieved in the transformer circuitry to be described below. Relay 58 is hermetically sealed and has a balanced armature so that it can operate in any position and can withstand substantial shock or vibration when the automobile is in use.

When the connection between capacitor C2 and line 54 is made via relay 58, unijunction transistor Q1 will act as an oscillator to provide positive output pulses in line 64 at a pulse rate which is controlled by the ratio of R1:C1 and at a pulse strength determined by the ratio of R2:R3. These pulses will charge the capacitor C3. Electrolytic capacitor C1 is connected directly between the common positive line 53 and the common negative line 54 to filter the circuitry from all static noise.

Resistor R1 and capacitor C2 are chosen such that at the input to transistor Q1 the pulses will be of saw tooth form. This will control the form of the pulses generated in the subsequent circuitry and the saw tooth pulse form is chosen since it is believed that it produces the most satisfactory operation of the pulsing circuitry. It should be stressed, however, that other pulse forms, such as square wave pulses, could be used. Capacitor C3 discharges through a resistor R4 to provide triggering signals for transistor Q2. Resistor R4 is connected to the common negative line 54 to serve as a gate current limiting device for transistor Q2.

The triggering signals produced by transistor Q2 via the network of capacitor C3 and a resistor R4 will be in the form of positive pulses of sharply spiked form. The collector of transistor Q2 is connected to the positive supply line 53 through resistor R6 while the emitter of that transistor is connected to the common negative line 54 through resistor R5. These resistors R5 and R6 control the strength of current pulses applied to a capacitor C4, which discharges through a resistor R7 to the common negative line 54, thereby to apply triggering signals to the gate of thyristor T1. The gate of thyristor T1 receives a negative bias from the common negative line via resistor R7 which thus serves to prevent triggering of the thyristor by inrush currents.

The triggering pulses applied to the gate of thyristor T1 will be very sharp spikes occurring at the same frequency as the saw tooth wave form pulses established by unijunction transistor Q1. It is preferred that this frequency be of the order of 10,000 pulses per minute and details of specific circuit components which will achieve this result are listed below. Transistor Q2 serves as an interface between unijunction transistor Q1 and thyristor T1, preventing back flow of emf from the gate of the thyristor which might otherwise interfere with the operation of transistor Q1. Because of the high voltages being handled by the thyristor and the high back emf applied to transistor Q2, the latter transistor must be mounted on a heat sink.

The cathode of thyristor T1 is connected via a line 65 to the common negative line 54 and the anode is connected via a line 66 to the centre of the secondary coil 67 of a first stage transformer TR1. The two ends of transformer coil 67 are connected via diodes D1 and D2 and a line 68 to the common negative line 54 to provide full wave rectification of the transformer output.

First stage transformer T1 has three primary coils 71, 72, 73 wound together with secondary coil 67 about a core 74. This transformer may be of conventional half cup construction with a ferrite core. The secondary coil may be wound on to a coil former disposed about the core and primary coils 71 and 73 may be wound in bifilar fashion over the secondary coil. The other primary coil 72 may then be wound over the coils 71, 73. Primary coils 71 and 73 are connected at one side by a line 75 to the uniform positive potential of circuit line 53 and at their other sides by lines 79, 81 to the collectors of transistors Q3, Q4. The emitters of transistors Q3, Q4 are connected permanently via a line 82 to the common negative line 54. A capacitor C6 is connected between lines 79, 81 to act as a filter preventing any potential difference between the collectors of transistors Q3, Q4.

The two ends of primary coil 72 are connected by lines 83, 84 to the bases of transistors Q3, Q4. This coil is centre tapped by a line 85 connected via resistor R9 to the positive line 53 and via resistor R10 to the common negative line 54.

When power is first applied to the circuit transistors Q3 and Q4 will be in their non-conducting states and there will be no current in primary coils 71, 73. However, the positive current in line 53 will provide via resistor R9 a triggering signal applied to the centre tap of coil 72 and this signal operates to trigger alternate high frequency oscillation of transistors Q3, Q4 which will result in rapid alternating pulses in primary coils 71, 73. The triggering signal applied to the centre tap of coil 72 is controlled by the resistor network provided by resistors R9 and R10 such that its magnitude is not sufficient to enable it to trigger Q3 and Q4 simultaneously but is sufficient to trigger one of those transistors. Therefore only one of the transistors is fired by the initial triggering signal to cause a current to flow through the respective primary coil 71 or 73. The signal required to hold the transistor in the conducting state is much less than that required to trigger it initially, so that when the transistor becomes conductive some of the signal applied to the centre tap of coil 72 will be diverted to the non-conducting transistor to trigger it. Wnen the second transistor is thus fired to become conductive, current will flow through the other of the primary coils 71, 73, and since the emitters of the two transistors are directly connected together, the positive output of the second transistor will cause the first-fired transistor to be shut off. When the current drawn by the collector of the second-fired resistor drops, part of the signal on the centre tap of coil 72 is diverted back to the collector of the first transistor which is re-fired. It will be seen that the cycle will then repeat indefinitely